



Docket No. . 1232-4421US1  
U.S. Serial No. 09/664,715

**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

Applicants: UEHARA et al.  
Serial No.: 09/664,715  
Filed : September 19, 2000  
For : WAFER PROCESSING APPARATUS, WAFER PROCESSING METHOD, AND SEMICONDUCTOR SUBSTRATE FABRICATION METHOD  
Group Art 1746  
Examiner: Unknown

**SUPPLEMENTAL TO SECOND INFORMATION DISCLOSURE STATEMENT**

Commissioner for Patents  
2900 Crystal Dr.  
Arlington, VA 22202-3513

**RECEIVED**

NOV 30 2001

Sir:

**TC 1700**

Applicants submit this Supplemental To Second Information Disclosure Statement to correct typographical errors contained in the PTO-1449 form filed on September 21, 2001. Specifically, EP3257826, EP1304733 and EP 8316182 should be JP3-257826, JP1-304733 and JP 8-316182 respectively.

A new PTO-1449 form is attached herewith to replace the PTO-1449 form filed on <sup>(paper no. 3)</sup> September 21, 2001. Copies of the references are not attached because they were submitted with the Second Information Disclosure Statement on September 21, 2001.

This document is being filed prior to a first Office Action. No fee is believed due by this filing.

The Commissioner is hereby authorized to charge any additional fees which may be

required for this Information Disclosure Statement, or credit any overpayment to Deposit

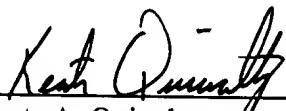
Account No. 13-4503, Order No. 1232-4421US1.

Respectfully submitted,

MORGAN & FINNEGAN, L.L.P.

Dated: November 29, 2001

By: \_\_\_\_\_

  
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